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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,612	07/17/2003	Eric T. Stubbs	M4065.0322/P322-A	9666

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,612	STUBBS ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-44 and 53-56* is/are pending in the application.

4a) Of the above claim(s) *1-33,45-52 and 57-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-44 and 53-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 21, 2006 has been entered.

2. Claims 34-44 and 53-56 are presented for examination. Claims 1-33, 45-52 and 57-59 have been cancelled.

3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

4. The rejection of claims 34-44 and 53-56 under 35 U.S.C. 112 first paragraph is hereby withdrawn due to amendment filed April 21, 2006.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 34-40 and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. (US Patent # 6,092,146) and Bosnyak (US Patent # 4,625,162).

With respect to claim 34, Dell et al. disclose:

a signaling circuit for encoding presence detect data comprising: a first signal encoding portion for encoding first presence detect information, said first presence detect information being disposed in a hard-wired circuit of an integrated circuit semiconductor memory device (figure 1, item 100) during the manufacturing of said integrated semiconductor memory device, said hard-wired circuit formed during manufacturing of said semiconductor memory device, by teaching in Table 1 in column 6 of serial presence detect (SPD) data being factory set;

and a second signal encoding portion for encoding second presence detect information said second information being disposed in a programmable circuit of said semiconductor memory device, said programmable circuit programmed subsequent to manufacturing of said semiconductor memory device, by teaching in Table 1 and the subsequent tables indicated therein for the

programming of particular SPD bytes;

wherein said second presence detect information is related to only said integrated circuit semiconductor memory device, by teaching in figure 1, that the presence detect bits in the PLD and EEPROM being related to device 100.

With respect to claim 35, Dell et al. disclose data relating to a storage capacity of said semiconductor memory device, as shown in Table 3.2 in column 7.

With respect to claim 36, Dell et al. disclose data relating to a data bus width of said semiconductor memory device, as shown by the data width sizes in Table 2.1.

With respect to claim 37, Dell et al. disclose data relating to a data access speed of said semiconductor memory device, as shown in Table 4.2 in column 7.

With respect to claim 38, Dell et al. disclose data relating to a column address strobe latency of said semiconductor memory device, as shown in Table 3.2 in column 7.

With respect to claim 39, Dell et al. disclose data relating to a data refresh rate of said semiconductor memory device, as discussed in column 5, lines 60+.

With respect to claim 40, Dell et al. disclose data relating to an interface voltage of said semiconductor memory device, as discussed in column 6, lines 5+.

With respect to claim 53, Dell et al. disclose:

receiving a first signal at a memory controller from said

memory integrated circuit (figure 1, item 100), said first signal encoding first presence detect information hardwired into said memory integrated circuit during manufacturing of said memory integrated circuit, by teaching in Table 1 in column 6 of serial presence detect (SPD) data being factory set;

and receiving a second signal at a memory controller from said memory integrated circuit, said second signal encoding second presence detect information programmed into said memory integrated circuit subsequent to manufacturing of said memory integrated circuit, by teaching in Table 1 and the subsequent tables indicated therein for the programming of particular SPD bytes.

With respect to claim 54, Dell et al. disclose receiving a control signal at said memory integrated circuit from said memory controller, said control signal being related to at least one of said first signal and said second signal, as shown in figure 4.

With respect to claim 55, Dell et al. disclose receiving an address signal at said memory integrated circuit from said memory controller, said address signal having a format related to at least one of said first signal and said second signal, as shown by the RAS and CAS signals in figure 4.

With respect to claim 56, Dell et al. disclose recognizing an identity of said memory integrated circuit at said memory controller based on said first and second signals, by teaching in Table 1 of using the SPD bytes to determine the memory type or

configuration type.

With respect to independent claims 34 and 53, Dell teaches all other limitations as discussed above, but fails to specifically disclose said first presence detect data having one of a first value associated with a short circuit within said hardwired circuit and a second value associated with an open circuit within said hardwired circuit. Bosnyak teaches in column 1, lines 24-30, that array bits are set to one of two logical states by either keeping the fuse for that bits intact (short circuit), or blowing the fuse to create and open circuit.

It would have been obvious to one of ordinary skill in the art, having the teachings of Dell *et al.* and Bosnyak before him at the time the invention was made, to modify the factory setting taught by Dell *et al.*, to instead be hardwired as in the conventional art of Bosnyak, in order to provide static settings, as taught by Bosnyak.

7. Claims 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. and Bosnyak.

With respect to claims 41, Dell et al. and Bosnyak teach all other limitations as discussed above, including wherein said first signal portion and said second signal portion comprise first and second serial data signals respectively, as shown in Table 1, but does not specifically disclose said first and second serial data signals being adapted to be transmitted over a single data line.

It would have been obvious to one of ordinary skill in the art, having the teachings of Dell *et al.* and Bosnyak before him at the time the invention was made, to modify the presence detect bits taught by Dell *et al.*, to be sent over a single data line in order to conserve chip space, as well known in the art.

With respect to claims 42-44, the difference between Dell *et al.* and Bosnyak and the claims is the claims recite the circuit being a fuse device, antifuse device, or a transistor-based device. However, the specific use of these particular device types does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter to one skilled in the art to utilize the circuitry of Dell *et al.* and Bosnyak with any of these types of devices in order to gain their benefits, since applicant has not disclosed that a particular device type, as opposed to other memory devices, overcomes a deficiency in the prior art or is for any stated purpose.

8. Claims 34-44 and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. and Bosnyak.

In addition to that discussed above, with respect to claims 34 and 53, assuming arguendo, the difference between Dell *et al.* and Bosnyak and the claims is the claims recite the presence detect data being stored on an integrated semiconductor memory

device. However, the specific use of an integrated device does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter to one skilled in the art to utilize the circuitry of Dell *et al.* and Bosnyak as an integrated semiconductor device, since applicant has not disclosed that a particular device type, as opposed to other memory devices, overcomes a deficiency in the prior art or is for any stated purpose. See also MPEP 2144.04 as to why making elements integral would be merely a matter of obvious engineering choice. Additionally, it would be obvious that if all elements are integrated, then the second presence detect bits would only be related to the integrated device itself.

9. Claims 34-44 and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al., Bosnyak, and Gowda et al. (US Patent # 6,275,259).

In addition to that discussed above, with respect to claims 34 and 53, assuming arguendo, the difference between Dell *et al.* and Bosnyak and the claims is the claims recite the first presence detect data being hardwired instead of factory set, as disclosed in Dell et al.. Gowda et al. though teaches in column 4, lines 28-34, that the factory setting of the present invention allows for the use of algorithms implemented in digital circuitry for the automatic gain control function.

It would have been obvious to one of ordinary skill in the art, having the teachings of Dell *et al.*, Bosnyak, and Gowda *et al.* before him at the time the invention was made, to modify the factory setting taught by Dell *et al.* and Bosnyak, to instead be hardwired as in the conventional art of Gowda *et al.*, in order to provide static settings, as taught by Gowda *et al.*.

10. Applicant's arguments filed 4/21/06 have been fully considered but they are not persuasive.

Response to Arguments

11. As per remark, Applicant's counsel asserts that (a) "the cited references do not disclose presence detect data related to a random access semiconductor memory chip wherein the presence detect data is either "disposed in a hardwired circuit of said random access semiconductor memory chip" or "disposed in a programmable circuit of said random access semiconductor memory chip." (amendment page 8, first paragraph); (b) Dell fails to show a random access semiconductor memory chip which include presence detect logic; Dell does not teach that its memory adapter is "a random access semiconductor memory chip" (amendment page 10 bridging page 11 et seq.); and (c) Bosnyak and Gowda fail to show the shortcomings of Dell (amendment's page 12-15).

With respect to (a); as being detailed above, Examiner would

like to emphasize that presence detect data is taught in TABLE 1 in column 6 of serial presence detect (SPD) data being factory set wherein the presence detect bits in the PLD and EEPROM ARE related to the device 100. Examiner would further emphasize that the hardwired presence detect bits in page 10, lines 28-29 correspond to those in lines 23-24, which clearly states that those presence detect bits are programmed. Therefore, it is clear that the claimed "hardwired" does NOT mean that the bits are not programmed, and will not be interpreted as such. Because "hardwired" is not limited to bits that are not programmed, the factory set bits in Dell are considered to be hardwired. Also see paragraph 8 above for arguments with respect to the presence detect data being stored on an integrated semiconductor memory device.

With respect to (b), note the Dell programmable logic deive 114 of the device 100; in addition, the Examiner maintains that the claimed "device" is an overly broad term that could indeed include the memory adapter 100 of Dell. Assuming arguendo that such is not true, the Examiner has repeated in paragraph 8 above that such would be obvious.

With respect to (c); in considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art. It has been held that the

test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed invention is expressly suggested in any one or all of the references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871. In addition, Examiner further recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Bosnyak, Gowda and Dell references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the Bosnyak and Gowda references were used to provide evidence of providing static settings by disclosing in column 1, lines 24-30 (Bosnyak) that array bits are set to one of two logical states by either keeping the fuse for that bits intact (short circuit), or blowing the fuse to create and open circuit; and column 4, lines 28-34 of Gowda's reference that the factory setting of his invention

allows for the use of algorithms implemented in digital circuitry for the automatic gain control function. The 35 USC § 103 rejection based on said combination is therefore deemed to be proper.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

TVT/July 07, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100